Yang, Chia-Hsiang; Chou, Chun-Wei; Hsu, Chia-Shen; Chen, Chiao-En
A systolic array based GTD processor with a parallel algorithm. (English) Zbl 1468.68030

Editorial remark: No review copy delivered.

MSC:
68M07 Mathematical problems of computer architecture
15A23 Factorization of matrices
68W10 Parallel algorithms in computer science
68W35 Hardware implementations of nonnumerical algorithms (VLSI algorithms, etc.)
94A12 Signal theory (characterization, reconstruction, filtering, etc.)

Full Text: DOI